

CLAIMS

What is claimed is:

- 1 1. A method for providing a sinker on a semiconductor device comprising the
2 steps of:
 - 3 (a) providing a substrate region;
 - 4 (b) providing a buried layer and an epitaxial (EPI) layer over the substrate
5 region;
 - 6 (c) etching a plurality of device structures in the EPI layer;
 - 7 (d) providing a slot in the semiconductor substrate that is in contact with the
8 buried layer and the substrate region;
 - 9 (e) oxidizing the slot except at the bottom of the slot; and
 - 10 (f) providing metal within the slot.
- 11 2. The method of claim 1 wherein the at least one metal providing step (f)
12 comprises the step of:
 - 13 (f1) filling the slot utilizing a metal that is provided on the surface of the EPI
14 layer that is of a thickness that is one-half the depth or width of the at least one slot.
- 15 3. The method of claim 1 wherein the at least one metal comprises a plurality of
16 metals.
- 17 4. The method of claim 3 wherein the plurality of metals comprises two metals, a

2 first metal covers one half the slot depth and a second metal fills the slot.

1 5. The method of claim 4 wherein the plurality of metals comprises three deposited
2 metals, wherein the first and second metal depositions fill the slot followed by a deposited
3 dielectric, wherein the dielectric has contacts opened above the slots and the third deposited
4 metal provides an interconnect layer wherein the third metal forms the contacts to a circuit and
5 the second deposited metal.

6 6. The method of claim 1 wherein the metal is provided utilizing chemical vapor
deposition.

7 7. The method of claim 1 wherein the metal is provided utilizing sputter
deposition.

8 8. The method of claim 1 wherein the sinker can be coupled to a collector or a
2 drain of a device to ensure lowest resistance.

9. A semiconductor device comprising:
2 a semiconductor substrate, the semiconductor substrate including a plurality of
3 device structures thereon, and a buried layer in the semiconductor substrate; and
4 an interconnect on the semiconductor substrate, the interconnect comprising at
5 least one slot provided in the semiconductor substrate and at least one metal within the slot,
6 wherein the at least one slot is oxidized everywhere except at the bottom of the slot, and the

7 interconnect forms a sinker to the buried layer.

1 10. The semiconductor device of claim 9 wherein the metal comprises a plurality of
2 metals.

1 11. The semiconductor device of claim 10 wherein the plurality of metals comprises
2 two metals, a first metal covers one-half of the slot and a second metal fills the slot.

1 12. The semiconductor device of claim 11 wherein the plurality of metals comprises
2 three metals, wherein the first and second metals fill the slot and the third metal provides an
3 interconnect layer.

1 13. A high voltage interconnect on a semiconductor substrate, the substrate
2 including a buried layer comprising:

3 a slot provided in the semiconductor substrate; and
4 at least one metal within the slot, wherein the at least one slot is oxidized
5 everywhere except at the bottom of the slot, and the interconnect forms a sinker to the buried
6 layer.

1 14. The interconnect of claim 13 wherein the metal comprises a plurality of metals.

1 15. The interconnect of claim 14 wherein the plurality of metals comprises two
2 metals, a first metal covers one-half of the slot and a second metal fills the slot.

1 16. The interconnect of claim 14 wherein the plurality of metals comprises three
2 metals, wherein the first and second metals fill the slot and the third metal provides an
3 interconnect layer.

1 17. The interconnect of claim 12 wherein the sinker can be coupled to a collector on
2 a drain of a device to ensure lowest resistance.
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1 18. The interconnect of claim 16 wherein the slot with oxide completely around the
2 three deposited layers is coupled to an emitter of a bipolar device which provides a high current
3 carrying connection to the emitter.
*P1
P2
P3
P4
P5
P6
P7
P8
P9
P10*

1 19. The interconnect of claim 16 wherein the slot with oxide completely around the
2 three deposited layers is coupled to a source MOS transistor which provides a high current
3 carrying connection to the source.
*P1
P2
P3
P4
P5
P6
P7
P8
P9
P10*

1 20. The interconnect of claim 16 wherein there are a plurality of slots filled with
2 three depositions of metal.

1 21. The interconnect of claim 20 wherein the plurality of slots are coupled to the
2 emitters, collectors, drains, sources of Bipolar transistors and MOS transistors on the same
3 device, thus forming high current carrying conductors on a same device while limiting the area
4 consumed on the surface to a maximum width of a slot.

- M* 1
22. The interconnect of claim 21 wherein the high current carrying conductors are
on the same level of metal resulting in thick metal obtained vertically in the substrate, while
3 limiting the space on the surface of the device and not requiring additional planarization.

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